The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

Claims 1-13 (Cancelled)

14. (New) A semiconductor device, comprising:

a semiconductor substrate having a semiconductor substrate main unit and a thin portion, the thin portion being thinner than the semiconductor substrate main unit such that a recessed portion is formed in the semiconductor substrate at the thin portion, the thin portion having at least one through hole formed therein; and

a through wiring including a first wiring formed on a first surface of the semiconductor substrate, a second wiring formed on a second surface opposite to the first surface, and a third wiring that fills the through hole, is formed along a wall surface of the recessed portion, and connects the first wiring and the second wiring.

15. (New) The semiconductor device according to claim 14 further comprising:

a first semiconductor element formed on the first surface of the semiconductor substrate having a gate electrode, a source electrode and a drain electrode; and

a second semiconductor element formed on the second surface of the semiconductor substrate having a gate electrode, a source electrode and a drain electrode,

wherein the through wiring connects at least one of the source electrode and the drain electrode of the first semiconductor element to at least one of the source electrode and the drain electrode of the second semiconductor element.

16. (New) The semiconductor device according to claim 14 further comprising:

another semiconductor substrate disposed under the semiconductor substrate;

a third semiconductor element formed on a first surface of the another semiconductor substrate facing the semiconductor substrate having a gate electrode, a source electrode, and a drain electrode,

wherein the through wiring of the semiconductor substrate is connected to at least one of the source electrode and the drain electrode of the third semiconductor element.

17. (New) The semiconductor device according to claim 15 further comprising:

an another semiconductor substrate disposed under the semiconductor substrate;

a third semiconductor element formed on a first surface of the another semiconductor substrate facing the semiconductor substrate having a gate electrode, a source electrode, and a drain electrode,

wherein the through wiring is connected to at least one of the source electrode and the drain electrode of the first semiconductor element, at least one of the source electrode and the drain electrode of the second semiconductor element, and at least one of the source electrode and the drain electrode of the third semiconductor element.

18. (New) The semiconductor device according to claim 14, wherein

the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and

the through hole being formed at a location corresponding to a connection part of the first sub-wiring and the second sub-wiring.

19. (New) The semiconductor device according to claim 14, wherein

the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and

the through hole being formed at an end part of the second sub-wiring.

20. (New) The semiconductor device according to claim 14, wherein

the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and

a plurality of the through holes formed under the second sub-wiring.

21. (New) The semiconductor device according to claim 14, wherein

the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and

a third wiring ~~is~~ formed on the wall surface of the recessed portion along a direction intersecting with the border.

22. (New) A method of producing a semiconductor device, comprising the steps of:

forming an etching stopper having at least one opening portion to become an opening on a first surface of the semiconductor substrate;

forming a first wiring on the first surface of the semiconductor substrate at a position to cover at least the opening portion; and

forming a thin portion that forms a recessed portion at a position corresponding to the opening portion in the semiconductor substrate and that has at least one through hole passing through the opening portion of the semiconductor substrate by etching the semiconductor substrate from a second surface opposite to the first surface of the semiconductor substrate so that the etching stopper remains

forming a second wiring on the second surface opposite to the first surface and a third wiring along a wall surface of the recessed portion that fills the through hole.